WEST BENGAL STATE UNIVERSITY

B.Sc. Honours 3rd Semester Examination, 2020, held in 2021

PHSACOR07T-PHYSICS (CC7)

DIGITAL SYSTEMS AND APPLICATIONS

Time Allotted: 2 Hours | Full Marks: 40

The figures in the margin indicate full marks.
Candidates should answer in their own words and adhere to the word limits as practicable.
Answers must be precise and to the point to earn credit.
All symbols are of usual significance.

Question No. 1 is compulsory and answer any *two* from the rest

1. Answer any ***ten*** questions from the following: 2×10 = 20

   (a) What are the advantages and limitations of ICs?

   (b) Why is delay line used in the vertical deflection system of a CRO?

   (c) What is the function of aquadag in a CRT?

   (d) Convert $(2598.675)_{10}$ to hexadecimal.

   (e) Perform the decimal addition 679.6 + 536.8 in the 8421 BCD code.

   (f) Prove the Boolean identity :

   $$AB + B\bar{C} + \bar{A}(B + C) + \bar{B}C + \bar{A}\bar{B}\bar{C} + ABC = \bar{A} + B + C$$

   (g) Given $\overline{AB} + \bar{A}B = C$, find $\overline{AC} + \bar{A}C$.

   (h) Realise XNOR gate using only NAND gates.

   (i) Draw the circuit diagram of a 4-bit subtractor.

   (j) What is the need of clocking a flip-flop?

   (k) What are the differences between ripple counter and parallel counter?

   (l) What do you mean by edge triggering and level triggering?

   (m) Find the number of flip-flops required for a MOD-5 counter.

   (n) What are the main functions of a Register?

2. (a) What do you mean by deflection sensitivity of a CRT? Deduce an expression for deflection sensitivity of a CRT using magnetic deflection. Why do you use a saw-tooth voltage in a CRO? 2+3+2

   (b) Design a full adder using NAND gates only. Steps of calculation in designing are required. 3

3. (a) Expand $A(\bar{A}+B)(\bar{A}+B+\bar{C})$ to maxterms and minterms. 3

   (b) Simplify the expression $F=(x\oplus y)\oplus(xy)$ and draw the simplified circuit. 2+1

   (c) A binary ripple counter is required to count up to $(16383)_{10}$. Find how many flip-flops are required. If the clock frequency is 8.192 MHz what is the frequency at the output of the MSB? 2+2

4. (a) On the CRO screen, the time base control is calibrated by 0.2 ms/div. One full cycle of the display covers 10 divisions on the time scale. Find the frequency of the input. 3

   (b) Convert D flip-flop to a J-K flip-flop and vice versa. 2+2

   (c) Draw a 4-bit serial-in, serial-out shift register using J-K flip-flops and show output stages. 3

5. (a) What is meant by the propagation delay in a counter? 2

   (b) Design an asynchronous mod-10 counter using J-K flip-flop. Show the output. 4

   (c) Reduce the expression $f=\sum m(0, 1, 2, 3, 5, 7, 8, 9, 10, 12, 13)$ using *K*-Map and implement the minimal expression using NAND gates. Show all intermediate steps. 4

N.B. : *Students have to complete submission of their Answer Scripts through E-mail / Whatsapp to their own respective colleges on the same day / date of examination within 1 hour after end of exam. University / College authorities will not be held responsible for wrong submission (at in proper address). Students are strongly advised not to submit multiple copies of the same answer script.*

——×——